

United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONED FOR PATENTS P.O. Rox. 150 Alexandra, Vicenia 22313-1450 www.uspia.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO	
10/769,805	02/03/2004	Keishi Tamura	1309.43490X00	9553	
	7590 12/29/2006 STANGER MALLIR & F	RRUNDIDGE P.C	EXAM	IINER	
MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C. 1800 DIAGONAL ROAD SUITE 370 ALEXANDRIA, VA 22314			PATEL, I	PATEL, HETUL B	
			ART UNIT	PAPER NUMBER	
			2186		
· · · · · · · · · · · · · · · · · · ·					
SHORTENED STATUTOR	Y PERIOD OF RESPONSE	MAIL DATE	DELIVER	DELIVERY MODE	
3 MO	TTHS 12/29/2006 PAPER		PER		

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

	Application No.	Applicant(s)				
	10/769,805	TAMURA ET AL.				
Office Action Summary	Examiner	Art Unit				
	Hetul Patel	2186				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>03</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
 Responsive to communication(s) filed on <u>17 November 2006</u>. This action is FINAL. 2b) ∑ This action is non-final. Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. 						
Disposition of Claims						
4) Claim(s) 1-7 is/are pending in the application. 4a) Of the above claim(s) is/are withdraw 5) Claim(s) 5 is/are allowed. 6) Claim(s) 1-4,6 and 7 is/are rejected. 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or Application Papers 9) The specification is objected to by the Examiner 10) The drawing(s) filed on is/are: a) acceed to the drawing sheet (s) including the correction of	relection requirement. r. epted or b) objected to by the Edrawing(s) be held in abeyance. See on is required if the drawing(s) is obj	e 37 CFR 1.85(a). ected to. See 37 CFR 1.121(d).				
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 11/17/2006.	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal Pa 6) Other:	te				

Application/Control Number: 10/769,805 Page 2

Art Unit: 2186

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

- 1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 17, 2006 has been entered and carefully considered.
- 2. Claims 1-2 and 6-7 are amended and none of the claims are cancelled or newly added. Therefore, claims 1-7 are pending in this application.
- 3. The indicated allowability of claims 1-4 and 6-7 are withdrawn in view of the newly discovered reference(s) to Ofer et al. (USPN: 6,209,059). Rejections based on the newly cited reference(s) follow.

Priority

4. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on September 29, 2003. It is noted, however, that applicant has not filed a certified copy of the Japanese Application 2003-337239 as required by 35 U.S.C. 119(b).

Art Unit: 2186

Information Disclosure Statement

5. The information disclosure statement (IDS) submitted on 11/17/2006 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the examiner.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

- 6. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
- 7. Claim 4 recites the limitation "said logical units" in lines 3 and 5. There is insufficient antecedent basis for this limitation in the claim. It is not clear whether it refers to the at least one first logical unit or the second logical unit or both.

Claim Objections

8. Claim 5 is objected to because of the following informalities:

The phrase "said <u>each</u> path information" in line 13 of claim 5 should be written as "said path information" since it appears to refer to only one path information. If it mean to refer more than one path information, then it is suggested to replace with "<u>each of</u> said path information".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 9. Claims 1-4 and 6-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Ofer et al. (USPN: 6,209,059) hereinafter, Ofer.

As per claim 1, Ofer teaches a system (i.e. the storage system 14 in Fig. 1) having a first controller (i.e. the host controller 21 in Fig. 2) of a virtualization system (i.e. the combination of 21 and 24 in Fig. 2) and a second controller (i.e. the disk controller 25 in Fig. 2) of a disk array system (i.e. 26 in Fig. 2), said second controller being coupled to said first controller (i.e. via buses 22 and 23 as shown in Figs. 1 and 2), said system performing data processing according to a request from a host device (i.e. the HOST a in Fig. 1), wherein said first controller conducts mapping such that relations between at least one first logical unit (i.e. MBOX LUN0- MBOX LUNn in Fig. 2) accessed by said host device and at least one intermediate logical device (i.e. 26a-26n in Fig. 1) are set, wherein said intermediate logical device is related to a second logical unit (i.e. 26a-26n in Fig. 1) of said second controller by a virtualization setting function (i.e. in the Ofer prior art, a logical device is virtual device which includes a range of storage area corresponding to a partial or entire physical device; e.g. see Col. 3, lines 41-44) of said first controller, wherein said first logical unit is related to a first logical unit number (LUN) (i.e. MBOX LUN0- MBOX LUNn in Fig. 2), and wherein said second

Art Unit: 2186

logical unit is related to a second LUN (i.e. 26a-26n in Fig. 1) (e.g. see Col. 3, lines 13-52 and Figs. 1-2).

As per claim 2, see arguments with respect to the rejection of claim 1. Claim 2 is also rejected based on the same rationale as the rejection of claim 1.

As per claim 3, Ofer teaches the claimed invention as described above and furthermore, Ofer teaches that the intermediate logical device (i.e. 26a-26n in Fig. 1) is constructed by arranging at least one level of a first memory (i.e. hard drives 26 shown in Fig. 2), and at least one level of a second memory (i.e. the memory 24 shown in Fig. 2) hierarchically arranged at a level above the at least one level of first memory, and wherein a memory device (i.e. the logical unit LUN0 in the disk device 26a1 in Fig. 2) in the second controller is mapped to the at least one level of first memory (e.g. see Fig. 2).

As per claim 4, Ofer teaches the claimed invention as described above and furthermore, Ofer teaches that the said first controller further comprises a plurality of said logical units (i.e. LUN0-8 in Fig. 2) which can be accessed from said host device (i.e. the HOST a in Fig. 1) through plural paths (i.e. by using different paths thru BUSES A and B, 22-23, different disk controllers, 25a-n, in Fig. 1) different from each other (for example, LUN0 can be accessed from the host via 27a->21a->22->25a->26 or via 27b->21a->23->25a->26; see Figs. 1-2), wherein each of said logical units is related to each of said at least one intermediate device (i.e. 26a-26n in Fig. 1).

As per claim 6, Ofer teaches a control method of a system (i.e. the storage system 14 in Fig. 1) having a first controller (i.e. the host controller 21 in Fig. 2) of a

Art Unit: 2186

virtualization system and a second controller (i.e. the combination of 21 and 24 in Fig. 2) and a second controller (i.e. the disk controller 25 in Fig. 2) of a disk array system (i.e. 26 in Fig. 2), said second controller being coupled to said first controller (i.e. via buses 22 and 23 as shown in Figs. 1 and 2), said control method performing data processing according to a request from a host device, comprising the steps of: wherein said first controller conducts mapping such that relations between at least one first logical unit (i.e. MBOX LUN0- MBOX LUNn in Fig. 2) accessed by said host device and at least one intermediate logical device (i.e. 26a-26n in Fig. 1) are set, wherein said intermediate logical device is related to a second logical unit (i.e. 26a-26n in Fig. 1) of said second controller by a virtualization setting function (i.e. in the Ofer prior art, a logical device is virtual device which includes a range of storage area corresponding to a partial or entire physical device; e.g. see Col. 3, lines 41-44) of said first controller, wherein said first logical unit is related to a first logical unit number (LUN) (i.e. MBOX LUN0- MBOX LUNn in Fig. 2), and wherein said second logical unit is related to a second LUN (i.e. 26a-26n in Fig. 1); obtaining path information to a memory device (i.e. 26a1 shown in Fig. 2) arranged in said second controller; and mapping said obtained path information to said intermediate logical device (i.e. 26a-26n in Fig. 1) connected to said at least one logical unit accessed by said host device (e.g. see Col. 3, lines 13-52 and Figs. 1-2).

As per claim 7, see arguments with respect to the rejection of claims 6. Claim 7 is also rejected based on the same rationale as the rejection of claim 6.

Application/Control Number: 10/769,805

Art Unit: 2186

Page 7

Allowable Subject Matter

10. Claim 5 is allowed.

11. The following is a statement of reasons for the indication of allowable subject matter: The prior arts of record fail to teach or suggest the limitation of having the path information obtaining means wherein the path information is recognized as path information to the same memory device when said obtained path information exists in plural.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Application/Control Number: 10/769,805

Art Unit: 2186

Page 8

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

H.B.Patel 12/07/2006 Hetul Patel Patent Examiner Art Unit 2186